V. Claims

We claim:

1. A method of generating a progressively corrected scan signal, the progressively corrected scan signal having a magnitude independent of spectral reflectance from a background near a target, comprising:

generating a baseline signal by sampling light reflected from the target and background before transmitting a light scan at the target;

generating a detected signal by receiving light reflected from the target and background while transmitting the light scan at the target; and

subtracting the baseline signal from the detected signal to form the progressively corrected scan signal.

2. The method of claim 1 wherein the target comprises a barcode.

3. The method of claim 1 wherein the target comprises a sample vessel.

4. The method of claim 1 wherein the transmitting the light scan at the target comprises transmitting a laser beam at the target.

5. The method of claim 4 wherein the transmitting a laser beam at the target comprises transmitting a red laser beam at the target.

6. The method of claim 1 wherein the subtracting step comprises inverting the baseline signal and summing the detected and inverted baseline signals.

7. The method of claim 6 further comprising passing the detected signal through a first resistor and the inverted baseline signal through a second resistor before the summing.

8. The method of claim 7 wherein the ratio of the first resistor to the second resistor comprises the ratio 1:3.

9. The method of claim 8 further comprising amplifying the baseline signal by a factor of three before the inverting.

10. The method of claim 1 further comprising generating a scan synchronization signal immediately before transmitting the light scan, and generating the baseline signal immediately after generating the scan synchronization signal.

11. A circuit for producing an average level independent output signal from an input signal subject to fluctuations in average level, comprising:

a sample signal generator comprising an input and an output, the sample signal generator input receiving a sample timing signal;

a sample-and-hold circuit comprising an input, an output, and a sample trigger, the sample-and-hold input receiving the input signal subject to fluctuations in average level, the sample trigger operatively coupled to the sample signal generator output; and

a voltage amplifier comprising an input and an output, the amplifier input operatively coupled to the sample-and-hold output, the amplifier output operatively coupled to the sample-and-hold input.

12. The circuit of claim 11 wherein the input signal comprises an optical detector output signal.

13. The circuit of claim 12 wherein the detector output signal represents light reflected from a target and a background during a scan period.

14. The circuit of claim 13 wherein the target comprises a barcode.

15. The circuit of claim 13 wherein the target comprises a sample vessel.

16. The circuit of claim 11 wherein the output signal has a baseline of about zero volts.

17. The circuit of claim 11 wherein the sample signal generator comprises a differentiator and a bipolar transistor, the differentiator comprising an input and an

output, the differentiator input comprising the sample signal generator input, the differentiator output operatively coupled to the bipolar transistor.

18. The circuit of claim 17 wherein the differentiator comprises a capacitor and a resistor, the capacitor comprising an input and an output, the resistor comprising a first and a second terminal, the capacitor input comprising the sample signal generator input, the capacitor output operatively coupled to the first resistor terminal to form the differentiator output.

19. The circuit of claim of 17 wherein the bipolar transistor comprises a NPN bipolar transistor, the NPN bipolar transistor comprising a base and a collector, the transistor base operatively coupled to the differentiator output, the transistor collector comprising the sample signal generator output.

20. The circuit of claim 19 wherein the transistor further comprises an emitter, the emitter operatively coupled to a positive DC voltage source.

21. The circuit of claim 11 wherein the sample-and-hold input comprises a positive and a reference input, the reference sample-and-hold input operatively coupled to ground, the positive sample-and-hold input receiving the input signal subject to fluctuations in average level.

22. The circuit of claim 11 wherein the amplifier input comprises a positive and a negative input, the positive amplifier input operatively coupled to ground, the negative amplifier input operatively coupled to the sample-and-hold output.

23. The circuit of claim 11 wherein the amplifier output is operatively coupled to the sample-and-hold input via a first and a second resistor in series, the average level independent output signal being generated at a point between the first and second resistors.

24. The circuit of claim 23 wherein the ratio of the first resistor to the second resistor comprises 3:1.

25. A system for generating and transforming information contained in light reflected from an optical scan transmitted at a target in the vicinity of a background to information contained in an electrical signal, comprising:

an optical timing detector for producing a scan synchronization signal, a laser for producing the optical scan in response to the scan synchronization signal, an optically sensitive scan detector for receiving and converting the reflected light into an electrical detector output signal, the detector output signal being subject to variations in DC offset due to spectral reflectance from the background, and a coupling circuit for presenting the scan detector output signal to a subsequent circuit;

the coupling circuit comprising a sample signal generator, the sample signal generator comprising an input and an output, the sample signal generator input receiving a sample timing signal, a sample-and-hold circuit, the sample-and-hold comprising an input, an output, and a sample trigger, the sample-and-hold input receiving the scan detector output signal, the sample trigger operatively coupled to the sample signal generator output, and a voltage amplifier, the amplifier comprising an input and an output, the amplifier input operatively coupled to the sample-and-hold output, the amplifier output operatively coupled to the sample-and-hold input.

26. The circuit of claim 25 wherein the sample timing signal comprises the scan synchronization signal.

27. The circuit of claim 25 wherein the amplifier output signal has a baseline of about zero volts.

28. The circuit of claim 25 wherein the sample signal generator comprises a differentiator and a bipolar transistor, the differentiator comprising an input and an output, the differentiator input comprising the sample signal generator input, the differentiator output operatively coupled to the bipolar transistor.

29. The circuit of claim 28 wherein the differentiator comprises a capacitor and a resistor, the capacitor comprising an input and an output, the resistor comprising a first and a second terminal, the capacitor input comprising the sample signal generator input, the capacitor output operatively coupled to the first resistor terminal to form the

differentiator output.

30. The circuit of claim of 29 wherein the bipolar transistor comprises a NPN bipolar transistor, the NPN bipolar transistor comprising a base and a collector, the transistor base operatively coupled to the differentiator output, the transistor collector comprising the sample signal generator output.

31. The circuit of claim 30 wherein the transistor further comprises an emitter, the emitter operatively coupled to a positive DC voltage source.

32. The circuit of claim 25 wherein the sample-and-hold input comprises a positive and a reference input, the reference sample-and-hold input operatively coupled to ground, the positive sample-and-hold input receiving the scan detector output input signal.

33. The circuit of claim 25 wherein the amplifier input comprises a positive and a negative input, the positive amplifier input operatively coupled to ground, the negative amplifier input operatively coupled to the sample-and-hold output.

34. The circuit of claim 25 wherein the amplifier output is operatively coupled to the sample-and-hold input via a first and a second resistor in series.

35. The circuit of claim 34 wherein the ratio of the first resistor to the second resistor comprises 3:1.